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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,907	07/09/2002	Xiaoning Nie	57265 (45107)	1262

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,907	NIE, XIAONING	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14,17 -24* is/are pending in the application.

4a) Of the above claim(s) *1-12, 15,16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14,17,18,20-24* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/05/02* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-12,15,16 have been canceled. Claims 13,14,17 -24 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13, 14 , 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Irwin et al. (5,841,771) in view of Inoue (5,146,558).

3. As to claim 13, Alpert disclosed a processor system (see fig.2) including at least

a) a program memory (main memory) (see the prefetch of instructions from main memory in col.5, lines 24-33).,

b) instruction reading means (prefetcher) for reading out the instruction form the memory (see the prefetch of instructions from main memory in col.5, lines 24-33).,

c) instruction decoding means (decoder 202) for decoding the instructions (see decoder in col.5, lines 31-33),

d) a plurality of executing units (203)(204)(205) operable in parallel of various instructions (see parallel execution in col.5, lines 38-41 , lines 62-63), and the instruction read out means (prefetcher) and the decoder jointly provided for all

execution units (see the prefetch and decoding of the instructions to the execution units in col.5, lines 31-51).

4. Alpert did not specifically show his first bus was slower than the second bus as claimed . However, Irwin taught a data processing system having a first bus (header) (see the fifth octet of header occupied 2 times the interval of one octet in 01.24, lines 60-67) which was at a lower rate than the second bus (see the 4 octets per 25.7ns in col.25, lines 9-13, see also the separate header bus and payload bus in fig.9):It would have been obvious to one of ordinary skill in the art to use Irwin in Albert for including the slower rate as claimed because the use of Irwing could provide the ability of Albert to adjust to different speed, and therefore, providing the capability to accept a predefined set of data flow, and one of ordinary skill in the art should be able to recognize the advantage of using variable rate as being disclosed by Irwing into Alpert in order to achieve the enhanced flexibility in speed, and in doing so, provided a motivation.

5. Alpert is used as primary reference because it showed clearly the plurality of execution units in parallel (see parallel execution' in col.5, lines 38-41 , lines 62-63) while Irwin is used for showing the slower bus.

6. Alpert's second execution unit was also used for executing only one special type of instruction (see the floating point instruction in execution unit [205]).

7. Alpert did not specifically show his first execution unit was used for executing all types of instructions as clamed. However, Inoue disclosed a system including an execution unit (GSP34010) for executing all instructions including both the general purpose and graphical instructions (see col.6, lines 26-33). It would have been obvious to one of ordinary skill inn the art to use Inoue in Alpert for including the execution unit for executing all types of instructions as clamed because the use of Inoue could provide Alpert the processing ability to accept different type of instructions based on a predefined set of application conditions , and it could be readily achieved by reconfiguring the processor of Inoue into Alpert with modified control attributes (e.g. the width of the processor bus etc.) so that the processor for executing all types of instructions could be recognized by Alpert. And because Alpert did taught his was used which was a suggestion of the need for including an execution for executing all types of instructions, such as , and in doing so , provided a motivation.

8. Alpert also included a first execution unit (203) from executing all possible instructions linteger instructions) and a second execution unit (205) for execute required by the execution units (see the data cache 206 in col.5, lines 48-53).

9. As to claim 14, Alpert also included a temporary storage for storing information only a few instructions (floating point instructions, see col.5, lines 37-50).

10. As to claim 20, 22, Irwing also included header and payload data (see the separate header bus and payload bus in fig.9), transmitter and 1/0 pods (see 01.22, 23, Table 1).

11. As to claim 21, Irwing also included i/o ports (see col.22, 23, Table 1).

12. As to claim 23, Alpert also included first data bus and second data bus (see the input and output connections to the execution units in fig.2) .

13. As to claim 24, Alpert's first execution unit also connected to a second bus (see the output connection from (204) while the second execution unit (205) was only connected to the second data bus (see fig.2).

14. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Irwin et al. (5,841,771) in view of Inoue (5,146,558) as applied to claim 13 above. and further in view of Berg (4,196,470).

15. As to claim 17, neither Alpert nor Irwin specifically showed the move instruction disclosed one instruction for move a data block as claimed. However, Berg transferring data block (e.g. see col.3, lines 38-46). It would have been obvious to one of ordinary skill in the art to use Berg in Albert for including move instruction as claims because the use of Berg could provide the control capability of Alpert to adapt to specific type of data transfer based on a predetermined instruction format, such as a move instruction, and therefore, increasing the adaptability of the execution unit of Alpert, and because Alpert did show an offset values for a data block to be transferred (see the byte boundary in col.10, lines 1-2), which was a suggestion of the

need of using an instruction for moving data block, and it could be achieved by configuring the control parameters to the move instruction (e.g. the transfer instruction type, and the instruction width) into Alpert so that move instruction was implementable in Alpert to achieve the enhance control, in doing so, provided a motivation.

16. As to claim 18, Alpert also included a storage or loading address of a data block to be stored or loaded, the amount od data elements, an offset value for storage or reading out (see the detailed references of the data line and size in the data cache memory in col.6, lines 39-67, col.7, lines 1-24, see also col.8, lines 21-42, col.9, lines 8-3 the byte boundary for the offset value in col.10, lines 1-2).

17. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the path leading to the first 'execution unit was temporarily deactivated by the instruction read out means via the decoding means if momentarily no instruction had to be executed by the first execution unit.

14. The prior ad made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Pepera et al. (5,027,317) is cited for the teaching of a processor executing any instructions (see col.3, lines 55-67);

b) Harriman, Jr. et al. (5,442,750) is cited for the background teaching in the header bus and the data bus (see col.3, lines 16-45).

18. Alpert et al. (5,559,986) , Irwin et al. (5,841,771) , Harriman, Jr. et al. (5,442,750) and Berg (4,196,470) were cited on the record in previous action, therefore, copies are not being provided herein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL N. PAN
PRIMARY EXAMINER